ABSTRACT OF THE DISCLOSURE

A device configured to recover and repeat source synchronous data. The device is configured to receive source synchronous data via a first interface and recover the received data utilizing a first clock signal which is generated to be approximately ninety degrees out of phase with the received clock signal. A second clock signal is generated to be in phase with the received source synchronous clock signal. The second clock signal is the utilized to select a newly generated clock signal and latched data for transmission in a source synchronous manner. The device is further configured to shift the phase of the generated first clock signal to be approximately ninety degrees out of phase with the received data signal.